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Information Disclosure Statement By Applicant	Applicant: Eaton et al.	Group Not yet assigned
(Use Several Sheets if Necessary)	Filing Date July 14, 2003	

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
HR	A	6,038,656	03.14.00	Martin et al.	712	211	
HR	B	5,752,070	05.12.98	Martin et al.	712	33	
HR	C	6,044,061	03.28.00	Aybay et al.	370	230	
HR	D	5,832,303	11.03.98	Murase et al.	710	36	

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
HR	E	Andrew Matthew Lines, <u>Pipelined Asynchronous Circuits</u> , June 1995, revised June 1998, pp. 1-37.
HR	F	Alain J. Martin, <u>Compiling Communicating Processes into Delay-Insensitive VLSI Circuits</u> , December 31, 1985, Department of Computer Science California Institute of Technology, Pasadena, California, pp. 1-16.
HR	G	Alain J. Martin, <u>Erratum: Synthesis of Asynchronous VLSI Circuits</u> , March 22, 2000, Department of Computer Science California Institute of Technology, Pasadena, California, pp. 1-143.
HR	H	U.V. Cummings, et al. <u>An Asynchronous Pipelined Lattice Structure Filter</u> , Department of Computer Science California Institute of Technology, Pasadena, California, pp. 1-8.
HR	I	Alain J. Martin, et al. <u>The Design of an Asynchronous MIPS R3000 Microprocessor</u> , Department of Computer Science California Institute of Technology, Pasadena, California, pp. 1-18.
HR	J	C.L. Seitz, <u>System Timing</u> , chapter 7, pp. 218-262.
HR	K	F.U. Rosemberger et al., <u>Internally Clocked Delay-Insensitive Modules</u> , IEEE Trans., Computers, vol. 37, no. 9, pp. 1005-1018, September 1998.
HR	L	U.S. Application 09/501,638, filed on February 10, 2000, entitled, <u>Reshuffled Communications Processes in Pipelined Asynchronous Circuits</u> .
HR	M	Lee et al., <u>Crossbar-Based Gigabit Packet Switch with an Input-Polling Shared Bus Arbitration Mechanism</u> , September 21, 1997, XVI World Telecom Congress Proceedings, Interactive Session 3 - Systems Technology & Engineering, pp. 435-441.
HR	N	Ghosh et al., <u>Distributed Control Schemes for Fast Arbitration in Large Crossbar Networks</u> , March 1994, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 2, No. 1, pp. 55-67.
Examiner	Date Considered	
<i>Heidi Kozashok</i>	02/19/04	

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.